

DOCKET NO. 01-C-086 (STMI01-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

**IN THE CLAIMS**

Please amend the claims as follows.

1. (Currently Amended) A method for fabricating an integrated circuit, comprising the steps of:

fabricating a portion of the integrated circuit, the portion comprising at least one active circuit area;

fabricating a redistribution metal layer over the at least one active circuit area;

depositing a polyimide layer over at least a portion of the redistribution metal layer; and

etching the polyimide layer to leave at least one portion of the redistribution metal layer open to receive at least one solder bump;

wherein fabricating the redistribution metal layer comprises fabricating a vertical plug in electrical connection with a metal pad associated with the active circuit area and depositing a metal layer in electrical connection with the vertical plug.

2. (Previously Presented) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises the step of:

fabricating at least one flat portion of the redistribution metal layer to receive the at least one solder bump.

DOCKET NO. 01-C-086 (STM101-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

3. (Previously Presented) A method for fabricating an integrated circuit, comprising the steps of:

fabricating a portion of the integrated circuit, the portion comprising at least one active circuit area;

fabricating a redistribution metal layer over the at least one active circuit area;

depositing a polyimide layer over at least a portion of the redistribution metal layer; and

etching the polyimide layer to leave at least one portion of the redistribution metal layer open to receive at least one solder bump;

wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises the steps of:

fabricating the active circuit area and an associated metal pad on a base substrate;

fabricating a vertical plug in electrical connection with the metal pad;

depositing an undoped silicon oxide layer on the active circuit area and on a portion of the metal pad;

depositing a phosphosilicate glass layer on the undoped silicon oxide layer;

depositing a silicon oxynitride layer over the phosphosilicate glass layer; and

depositing a flat metal layer over the silicon oxynitride layer and in electrical connection with the vertical plug.

DOCKET NO. 01-C-086 (STM101-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

4. (Previously Presented) The method as set forth in Claim 3, wherein depositing the polyimide layer and etching the polyimide layer comprise the steps of:

depositing the polyimide layer over at least one portion of the flat metal layer and over at least one portion of the silicon oxynitride layer; and

etching at least one portion of the polyimide layer to leave at least one portion of the flat metal layer open to receive the at least one solder bump.

DOCKET NO. 01-C-086 (STMI01-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

5. (Previously Presented) A method for fabricating an integrated circuit, comprising the steps of:

fabricating a portion of the integrated circuit, the portion comprising at least one active circuit area;

fabricating a redistribution metal layer over the at least one active circuit area;

depositing a polyimide layer over at least a portion of the redistribution metal layer; and

etching the polyimide layer to leave at least one portion of the redistribution metal layer open to receive at least one solder bump;

wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises the steps of:

fabricating the active circuit area and an associated metal pad on a base substrate;

depositing an undoped silicon oxide layer on the active circuit area and on at least a portion of the metal pad;

depositing a phosphosilicate glass layer on the undoped silicon oxide layer;

depositing a metal layer over the phosphosilicate glass layer and in electrical connection with the metal pad; and

depositing a silicon oxynitride layer over at least some portions of the metal layer.

DOCKET NO. 01-C-086 (STMI01-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

6. (Previously Presented) The method as set forth in Claim 5, wherein depositing the polyimide layer comprises the step of:

depositing the polyimide layer over at least a portion of the silicon oxynitride layer.

7. (Previously Presented) The method as set forth in Claim 5, wherein depositing the silicon oxynitride layer comprises the step of:

depositing a silicon oxynitride layer over all portions of the metal layer.

8. (Previously Presented) The method as set forth in Claim 7, further comprising the step of:

etching the silicon oxynitride layer to a pattern that leaves at least one portion of the metal layer uncovered to receive the at least one solder bump.

9. (Previously Presented) The method as set forth in Claim 5, wherein depositing the polyimide layer and etching the polyimide layer comprise the steps of:

depositing the polyimide layer over at least one portion of the metal layer and over at least one portion of the silicon oxynitride layer; and

etching at least one portion of the polyimide layer to leave at least one portion of the flat metal layer open to receive the at least one solder bump.

**DOCKET NO. 01-C-086 (STMI01-01086)**  
**U.S. SERIAL NO. 10/091,743**  
**PATENT**

10. (Previously Presented) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises the step of:

fabricating the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

Claims 11-30 (Cancelled).

31. (Previously Presented) The method of Claim 1, further comprising:  
depositing a silicon oxynitride layer over the at least one active circuit area;  
wherein the redistribution metal layer is fabricated over the silicon oxynitride layer.

32. (Previously Presented) The method of Claim 31, wherein depositing the polyimide layer comprises:

depositing the polyimide layer over at least one portion of the redistribution metal layer and over at least one portion of the silicon oxynitride layer.

33. (Previously Presented) The method of Claim 1, further comprising:  
depositing a silicon oxynitride layer over at least a portion of the redistribution metal layer.

DOCKET NO. 01-C-086 (STMI01-01086)  
U.S. SERIAL NO. 10/091,743  
PATENT

34. (Previously Presented) The method of Claim 33, wherein depositing the polyimide layer comprises:

depositing the polyimide layer over at least one portion of the redistribution metal layer and over at least one portion of the silicon oxynitride layer.

35. (Previously Presented) The method of Claim 33, wherein depositing the silicon oxynitride layer comprises:

depositing a silicon oxynitride layer over all portions of the metal layer.

36. (Previously Presented) The method of Claim 35, further comprising:  
etching the silicon oxynitride layer to a pattern that leaves at least one portion of the redistribution metal layer uncovered to receive the at least one solder bump.

37. (Previously Presented) The method as set forth in Claim 3, wherein fabricating the redistribution metal layer comprises the step of:

fabricating at least one flat portion of the redistribution metal layer to receive the at least one solder bump.

**DOCKET NO. 01-C-086 (STMI01-01086)**  
**U.S. SERIAL NO. 10/091,743**  
**PATENT**

38. (Previously Presented) The method as set forth in Claim 3, wherein fabricating the redistribution metal layer comprises the step of:

fabricating the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

39. (Previously Presented) The method as set forth in Claim 5, wherein fabricating the redistribution metal layer comprises the step of:

fabricating at least one flat portion of the redistribution metal layer to receive the at least one solder bump.

40. (Previously Presented) The method as set forth in Claim 5, wherein fabricating the redistribution metal layer comprises the step of:

fabricating the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.